

# High DR ADC for LHC

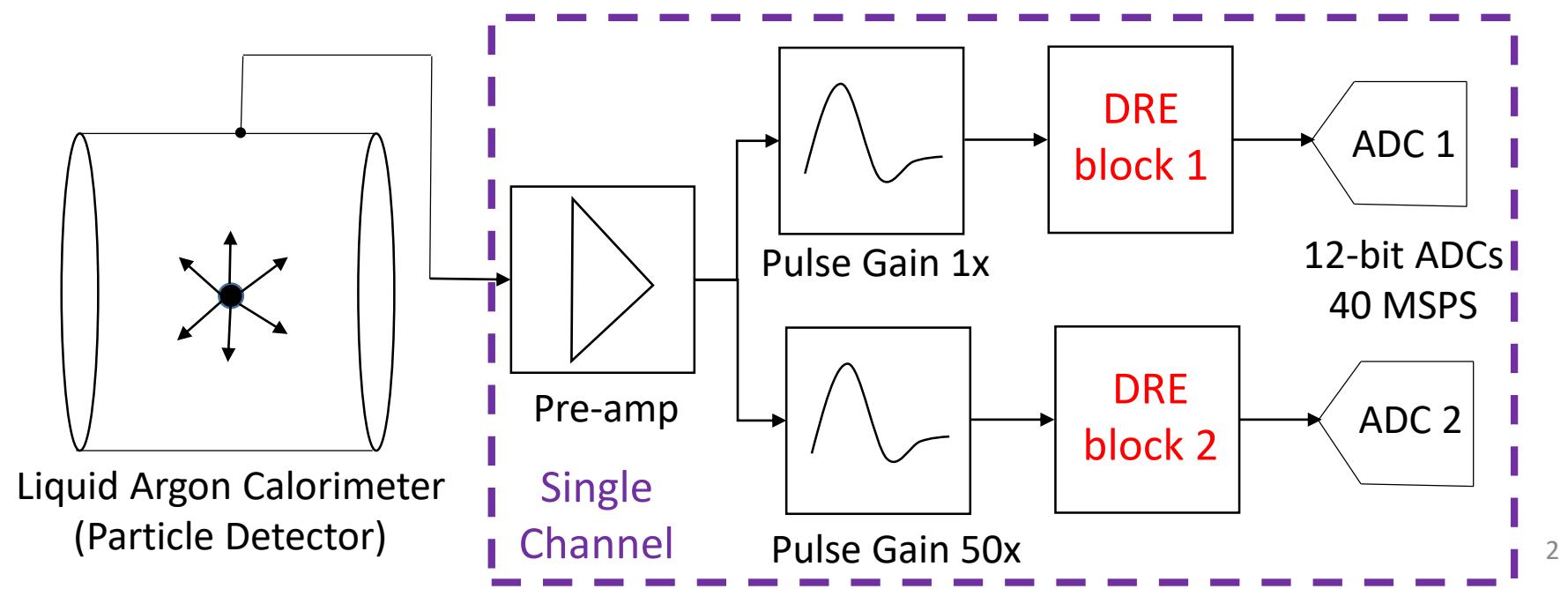
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# Aim: ADC design for The LHC (Large Hadron Collider), CERN

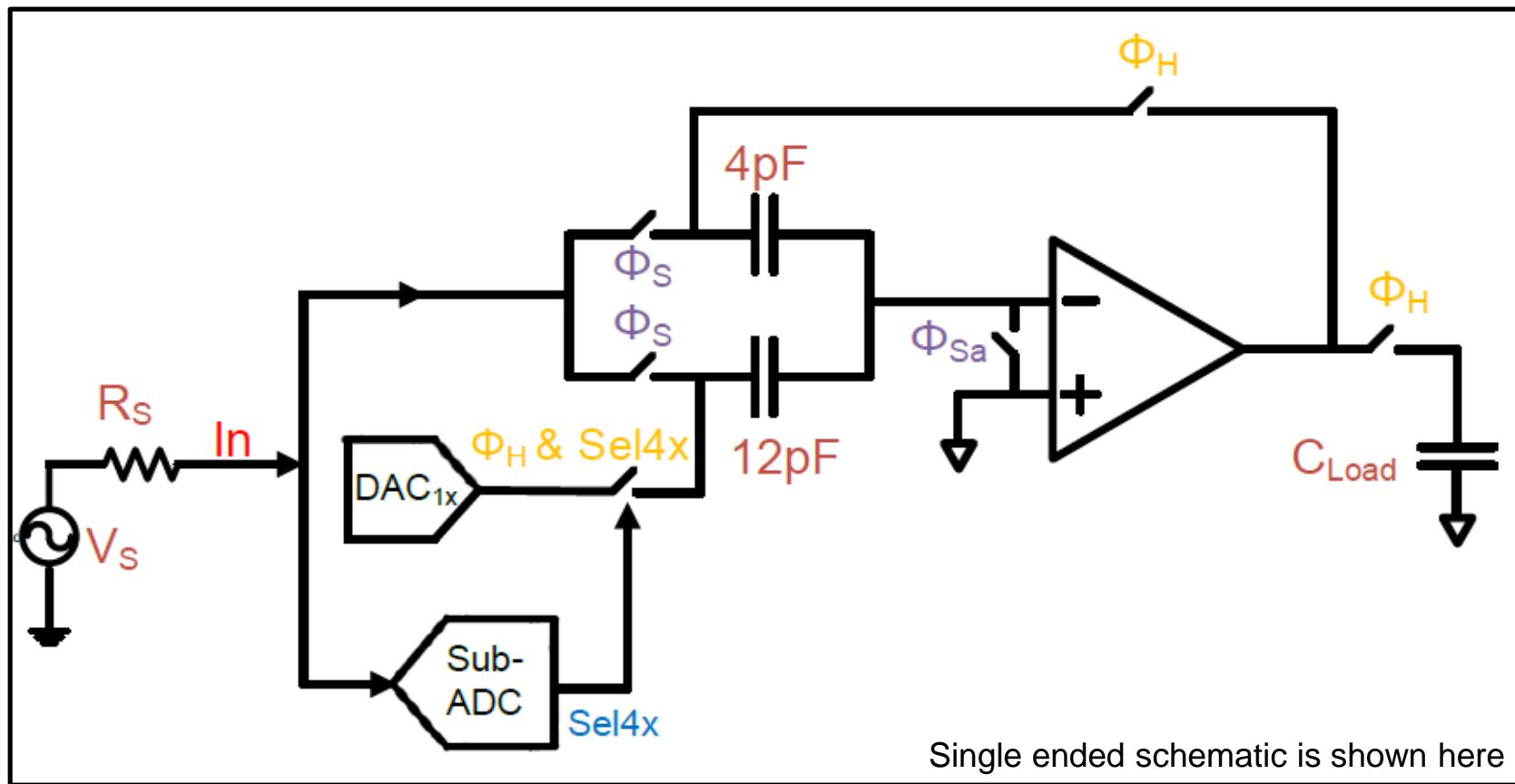
- ADC specifications:
  - 14-bit design: To accommodate high dynamic range (16 bit)
  - 40MSps
- To design: intermediate block
  - Increase accuracy to 14 bit (or enhance the dynamic range)



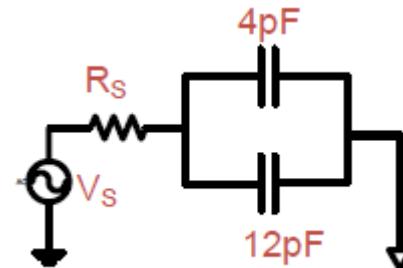
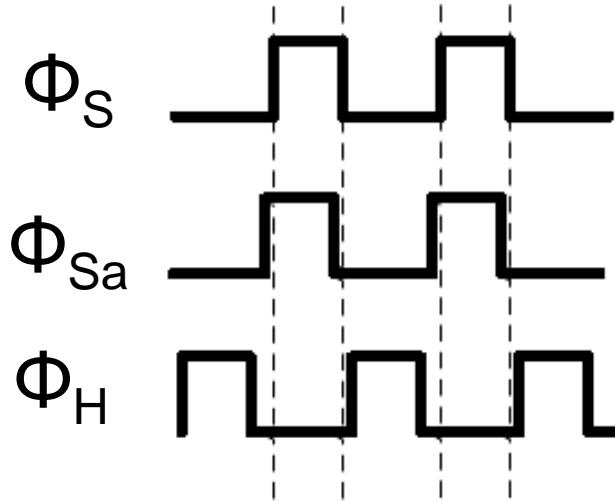
# Alternate topology: Sampling Amplifier (SA) based DRE

Small input: 4x gain

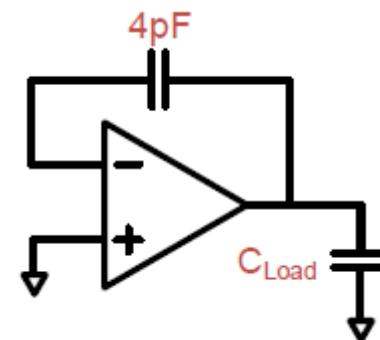
Large input: 1x gain



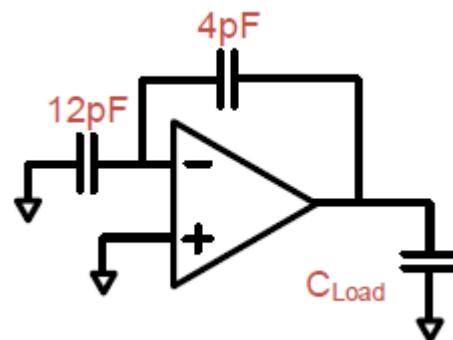
# SA-DRE timing diagram



Sample Phase



Hold Phase &  
1x Selected



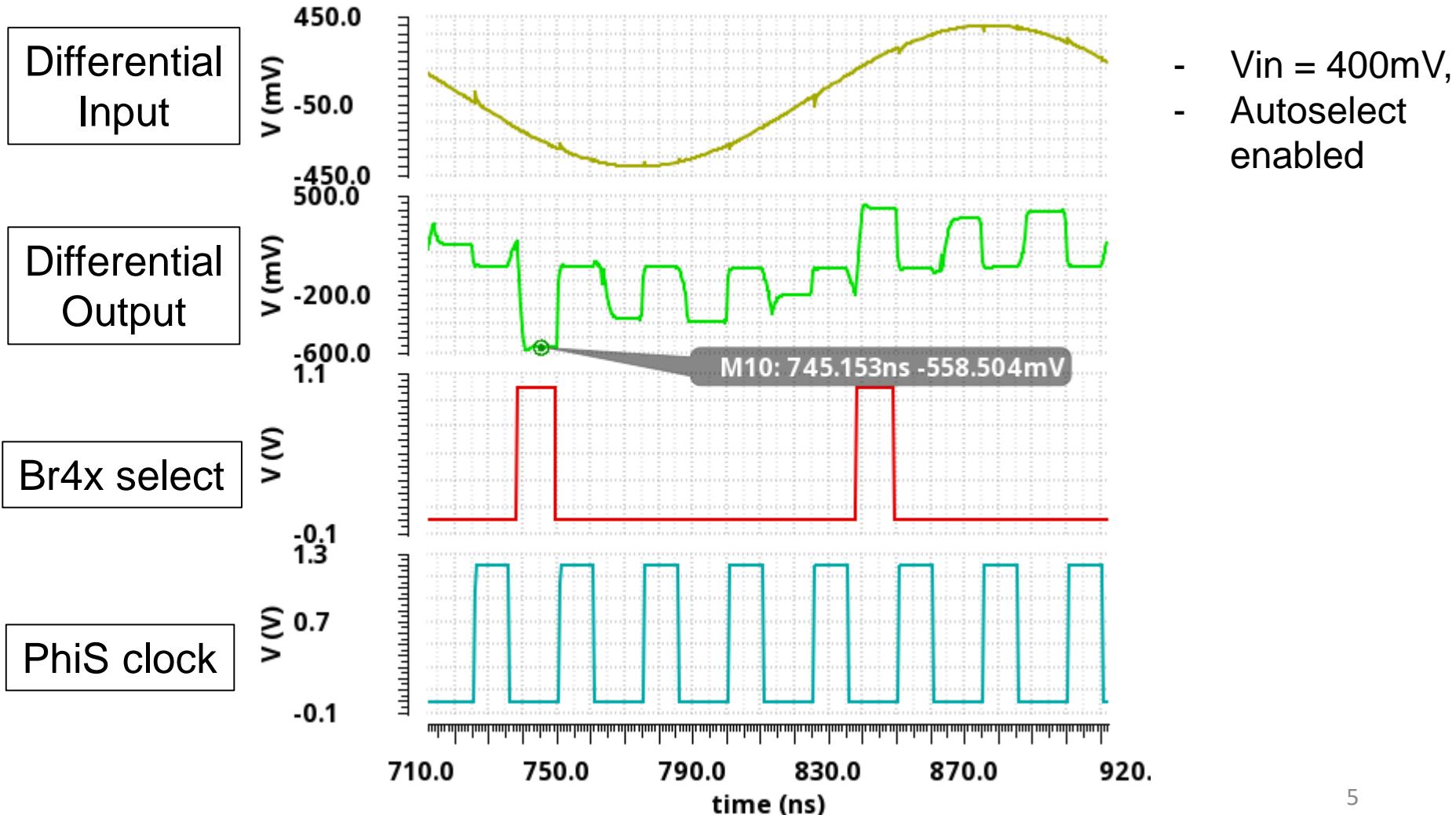
Hold Phase &  
4x Selected

Sample (11.5nsec)      Amplify (11.5 nsec)

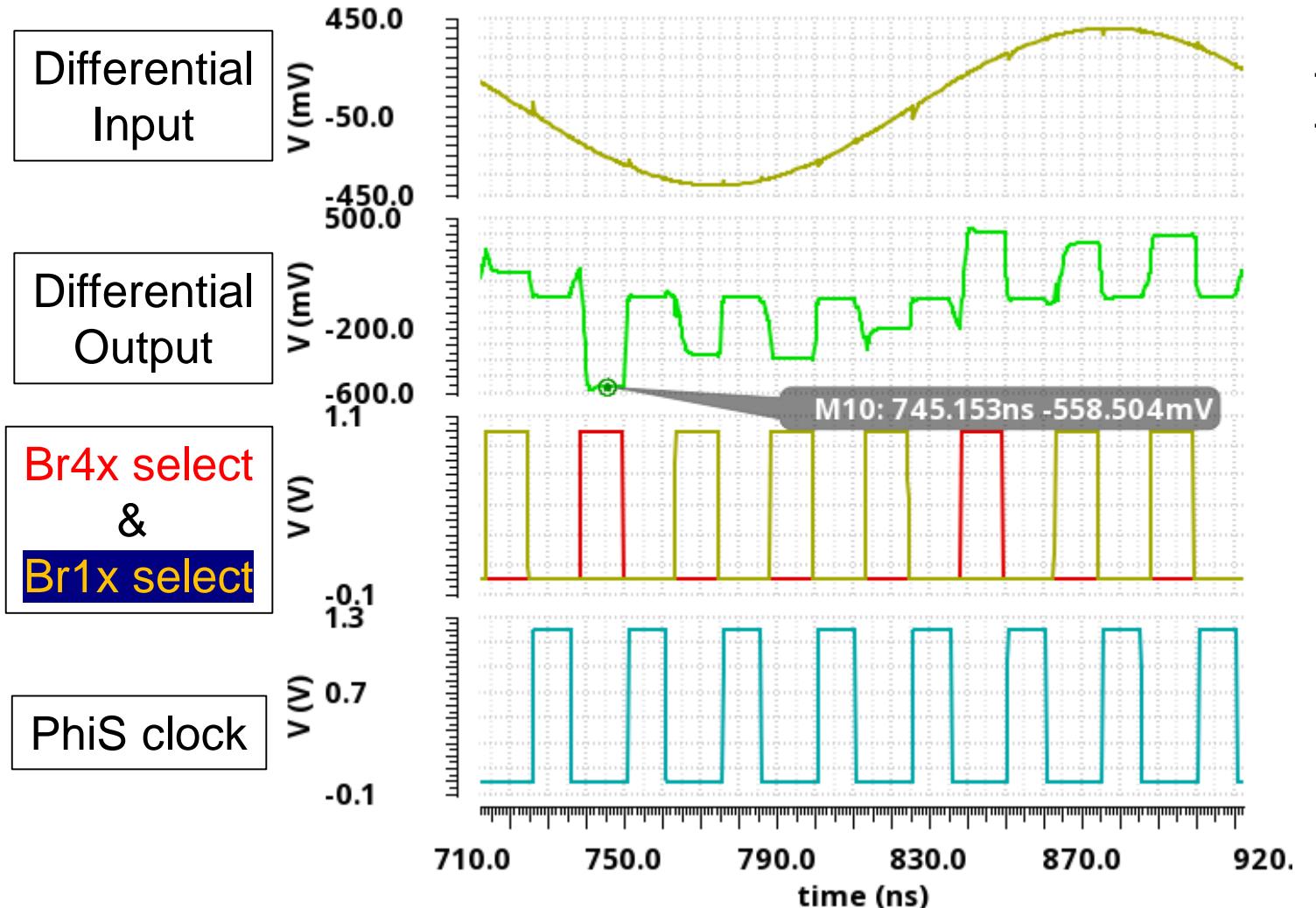
Decide(2nsec)

$T_{CLK} = 25\text{nsec}$

# Auto select timing diagram

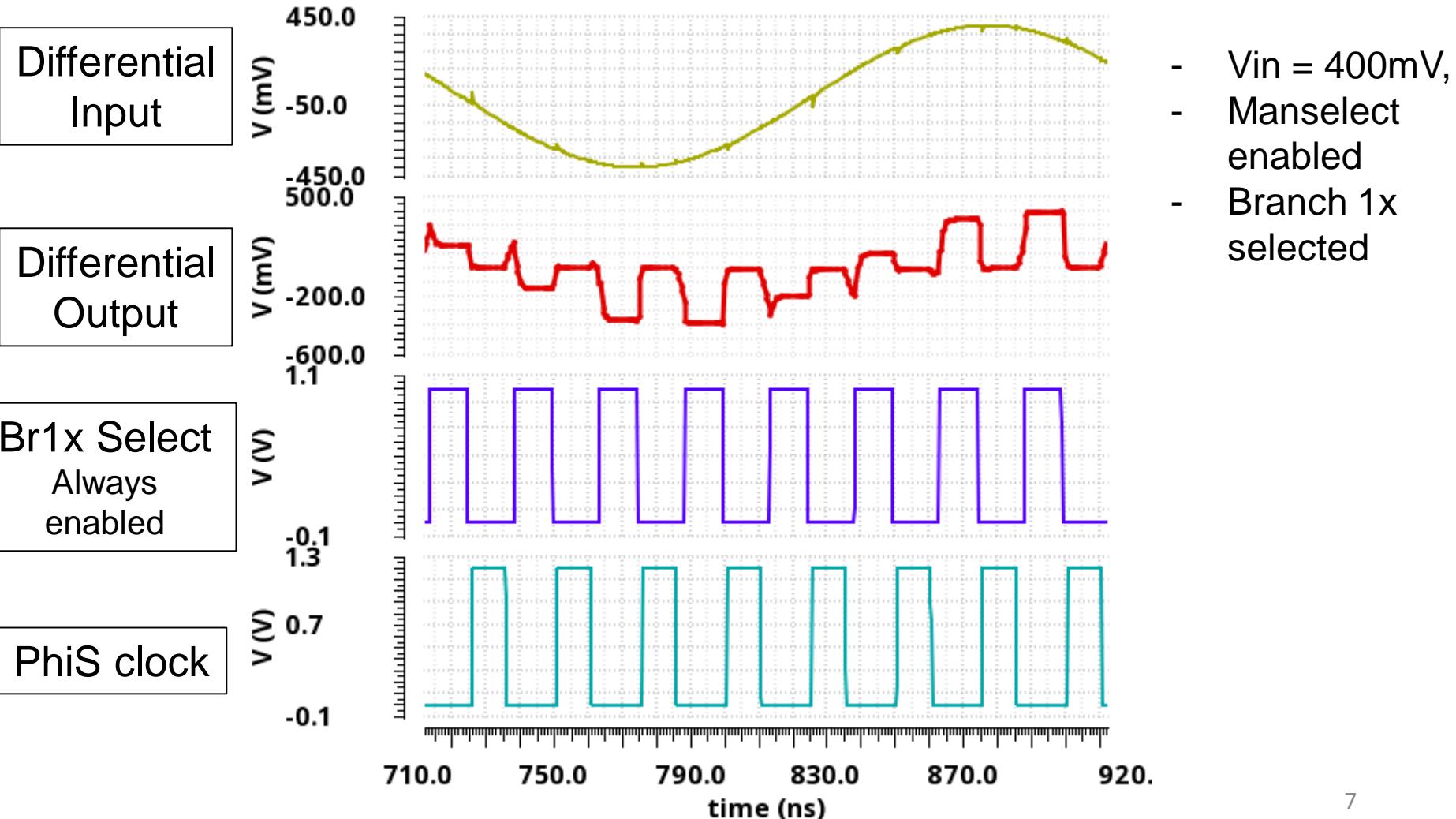


# Auto select timing diagram



- $V_{in} = 400\text{mV}$ ,
- Autoselect enabled

# Manual select timing diagram

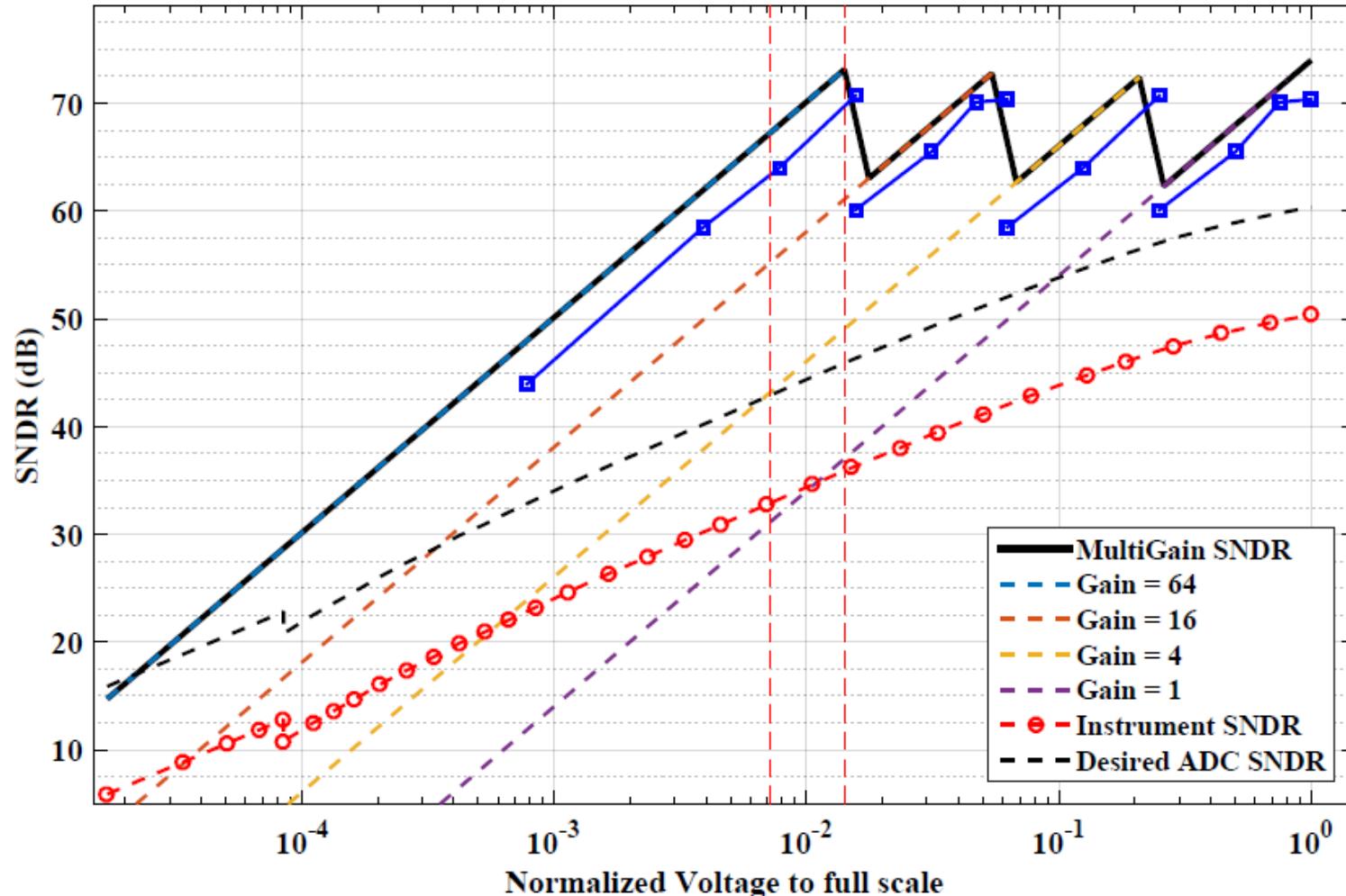


# Sim Results@ 5MHz Input, 40MSPS

- 1.6V<sub>pp</sub> differential input provided, 1x gain selected manually.
  - Similar results obtained for using 4x gain at maximum value.
- Simulations contain:
  - Transistor level transient simulation
  - Transient noise enabled
  - Input resistance of 10Ω. Bond wires not added yet.
- Tt, ff, ss, sf and fs corners simulated for 0°C and 50°C
  - All results better than 68.7dB SNDR
  - **Bias currents not adjusted yet** to equalize power consumption.

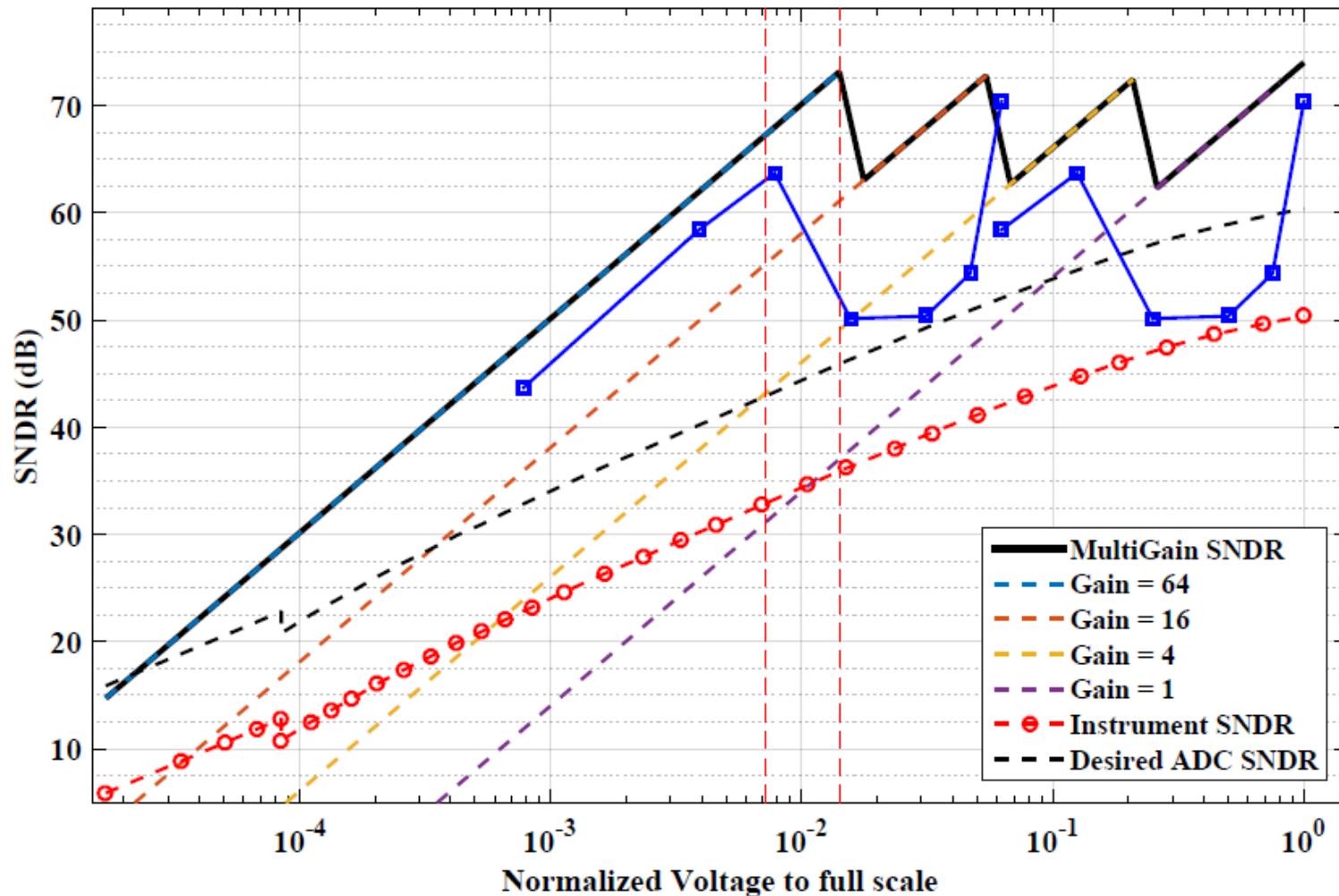
Corner	SNR (dB)	SNDR (dB)	Current (mA)	Vout <sub>pp</sub> (diff) (V)
tt 0	73.1	70.58	13.83	1.6
tt 50	72.38	68.7	14.6	1.6
ss0	72.33	70.7	11.96	1.6
ff 50	71.77	69.27	20.16	1.6

# Current Status: With ManSel: ss0



- Manual select means either one of 1x gain or 4x gain is selected for the complete experiment .

# Current Status: With AutoSel: ss0

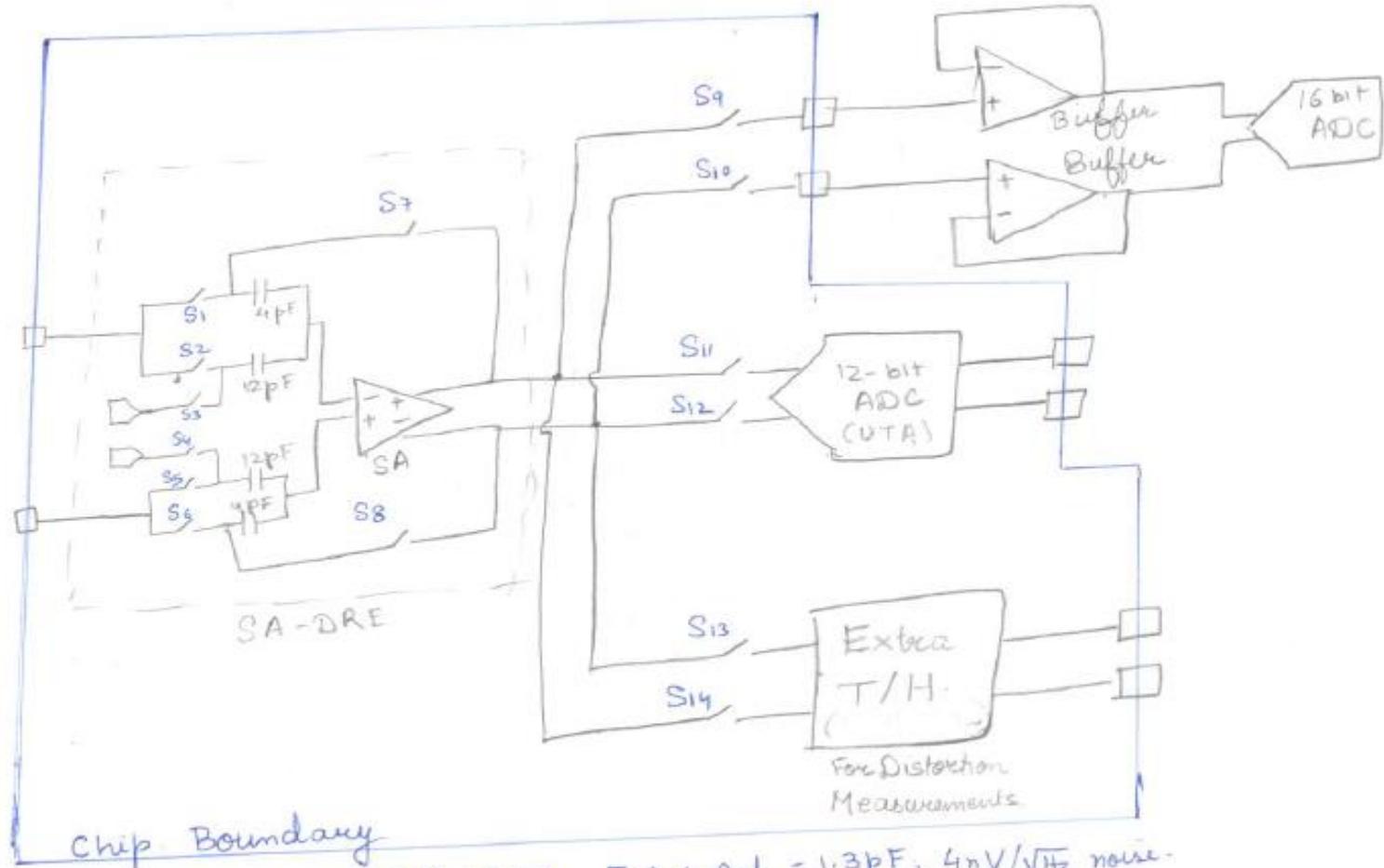


- Auto select means verilogA logic block determines whether to choose 1x gain or 4x gain, based on input.

# Auto Select SNDR: Comments

- Data points indicate a shift by  $\sim 12\text{mV}$  in 4x branch compared to 1x branch
- When expected output = 0V, output  $\sim 12\text{mV}$ 
  - Max SNDR limited to 52dB or so
- Full Scale input ( $V_{FS}$ ): Fast switching, 4x sample is never used.
  - Because 4x branch has to be enabled for atleast 2 samples before using its sample
  - Therefore full scale input follows 1x output  $\rightarrow 70\text{dB}$  SNDR
- Working on finding reason for offset

# PCB level schematic

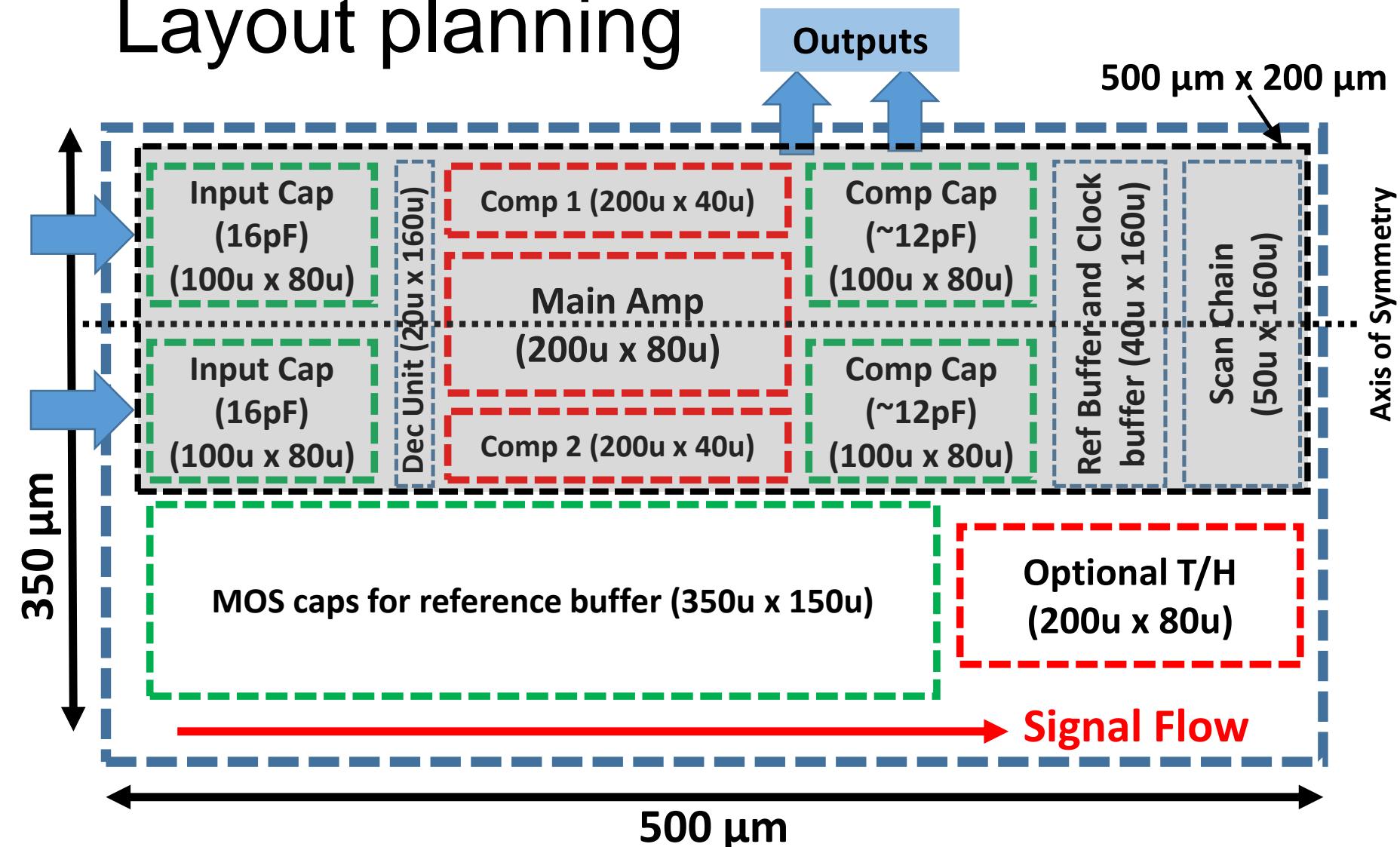


Chip Boundary

External Buffer = ADA 4817, Input cap =  $1.3\text{pF}$ ,  $4\text{nV}/\sqrt{\text{Hz}}$  noise.

External ADC = AD 9650, 1.8 V supply ~~2.7 V~~  $\text{pp}$  output,  
~~83 dB SNDR~~ 83 dB SNDR, 25 MSPS to 105 MSPS

# Layout planning



Channel area:  $500 \mu\text{m} \times 200 \mu\text{m}$ , Active area:  $500 \mu\text{m} \times 350 \mu\text{m}$

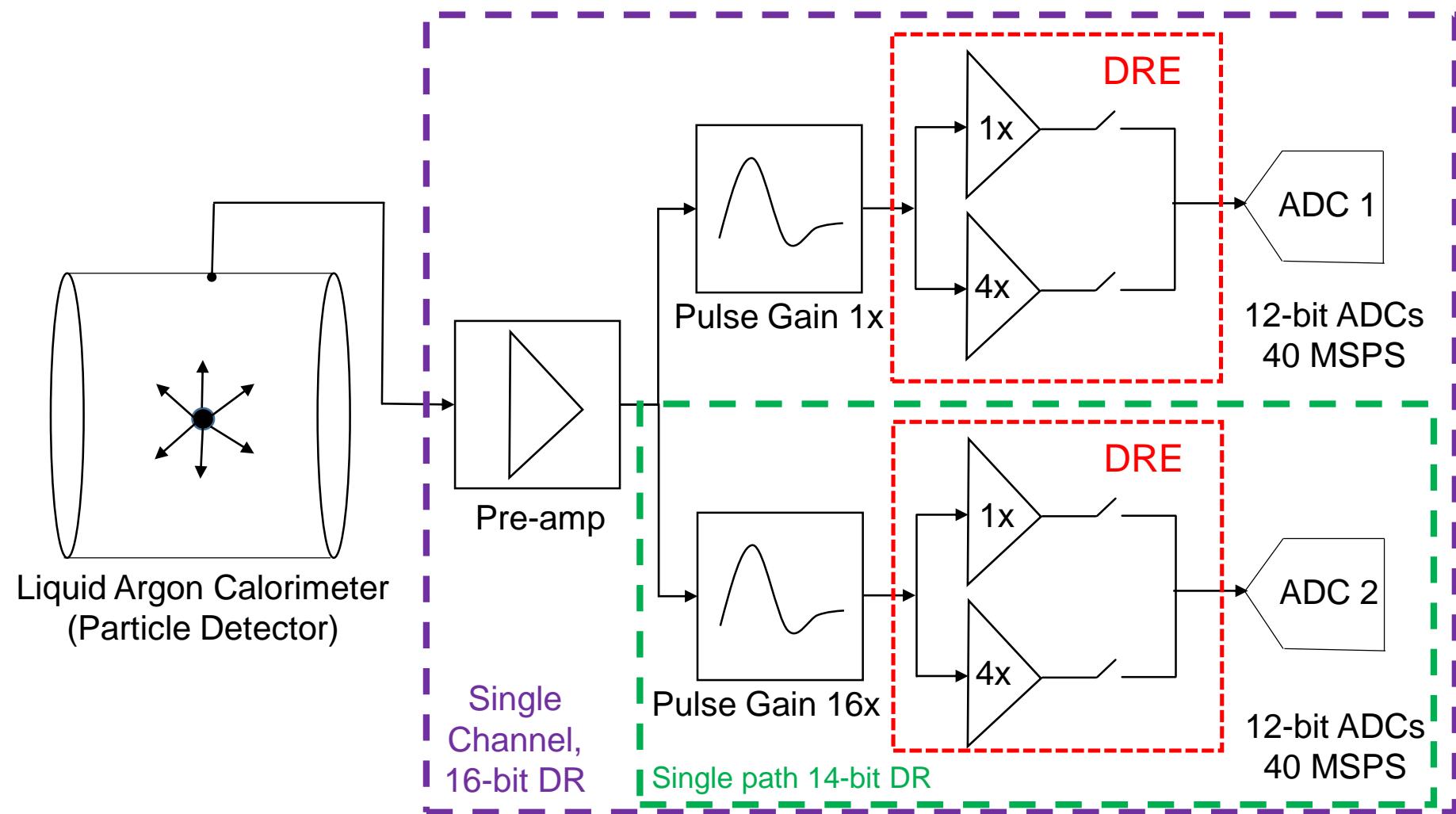
# Next steps and Timeline

- Complete block level simulations
  - Debug autoselect output
  - Layout, PEX etc.
- If time permits:
    - Low frequency T&H
    - Implement calibration scheme in Matlab

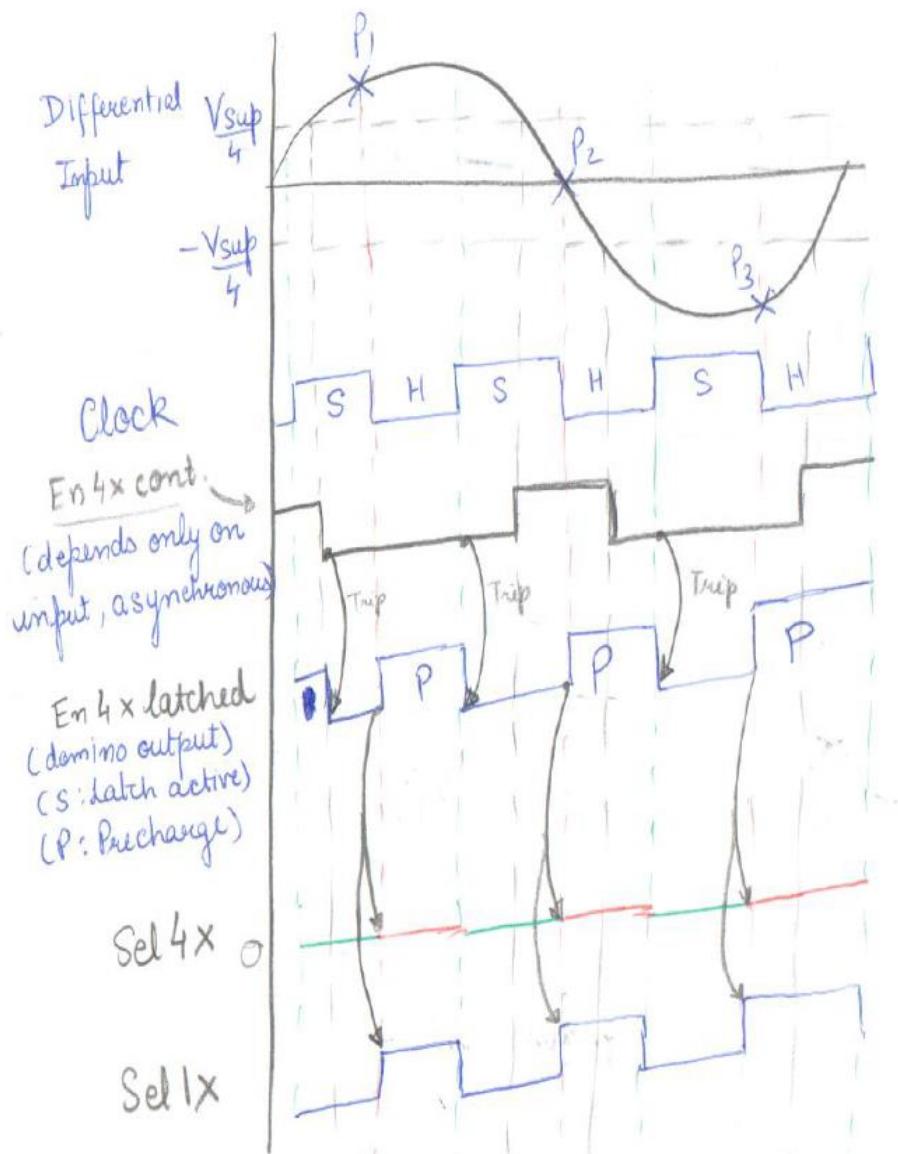
S.No.	Item	Complete by
1	Schematics upto pcb level (except T&H)	Mar 22 <sup>nd</sup> , 2017
2	Layout of individual blocks	Apr 5 <sup>th</sup> , 2017
3	Top level routing, pad connections	Apr 13 <sup>th</sup> , 2017
4	PEX, functionality test	Apr 20 <sup>th</sup> , 2017

# Backup Slides

# Dual gain as DRE



# Switching selection scheme (contd.)



## Timing

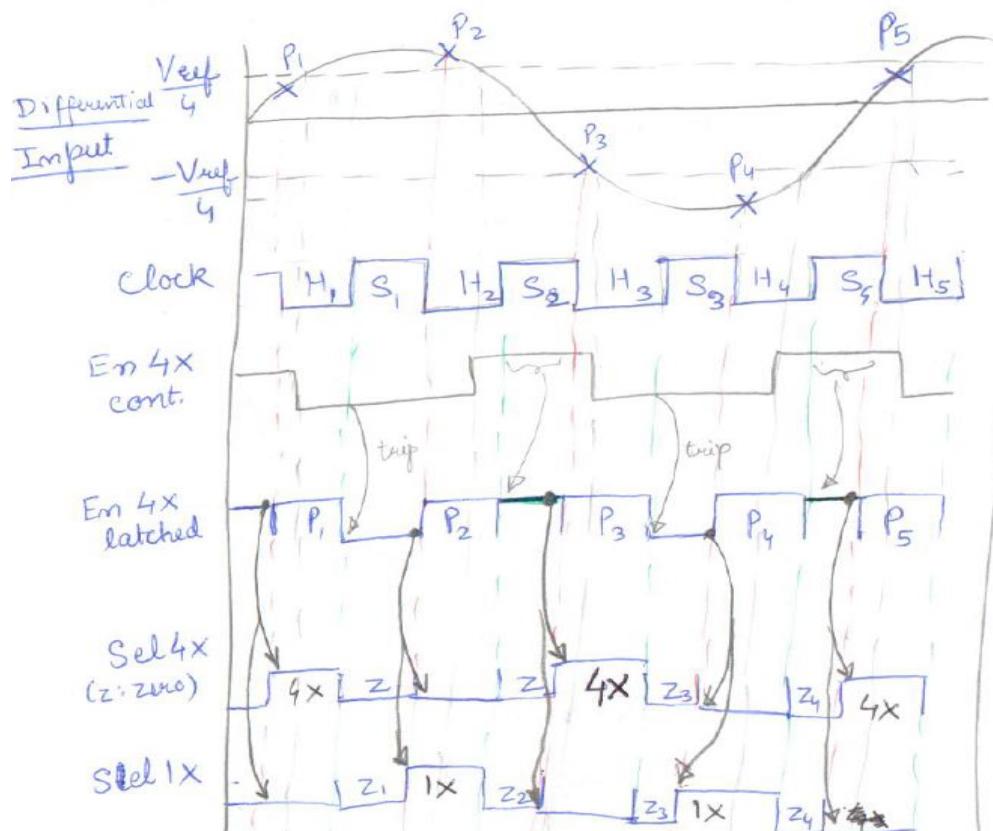
- S  $\Rightarrow$  1x & 4x sample
- Hadv  $\Rightarrow$  Decide 1x or 4x
- H  $\Rightarrow$  Either sel 1x or sel 4x becomes 1.

## Selection process:

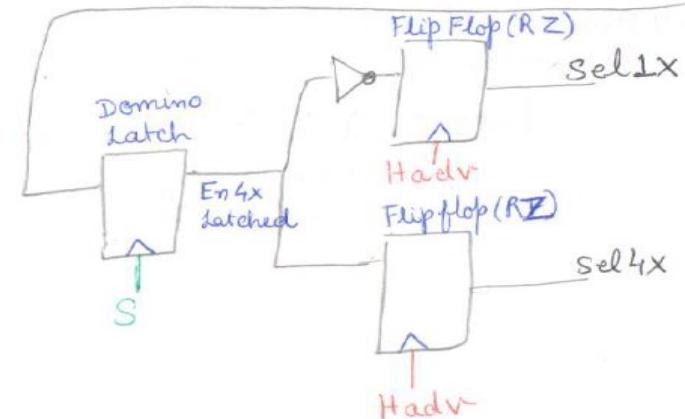
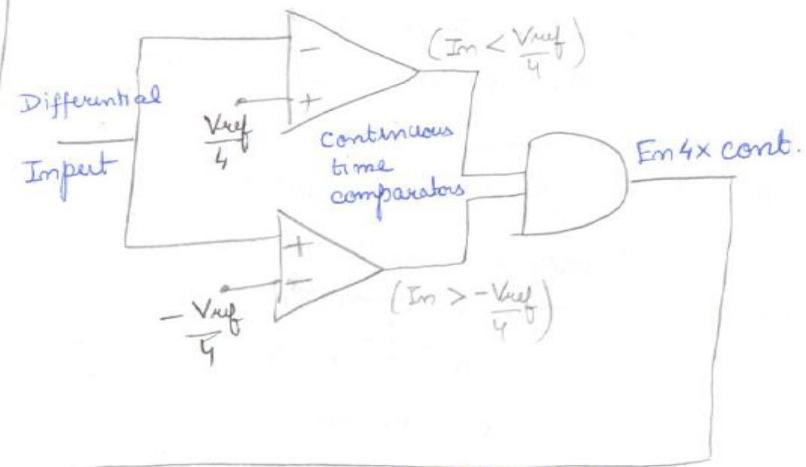
- H  $\Rightarrow$  Precharge (P) En4x latched node (output of domino latch)
- S  $\Rightarrow$  Latch active, anytime En4x cont. is 0(zero), domino trips, output 0.
- Hadv  $\Rightarrow$  Transfer latch value to make either sel 1x active or sel4x active
- H  $\Rightarrow$  cycle repeats
- During S, sel1x & sel4x are 0(zero)

# Switching selection scheme (contd.)

Case 2: Smaller input



Circuit Diagram:



Continuous time comparators: High gain fast amplifiers (40 dB)